VeriTiger®-V9P

HyperSilicon® 亞科鴻禹

VeriTiger®-V9P is a pretty agile and easy bring-up prototyping system from HyperSilicon, using Xilinx Virtex UltraScale+ XCVU9P FPGA. VeriTigerV9P delivers high performance, fast running speed and flexible scalability to accelerate software development, system verification and validation. Through the Protowizard® software to manage prototyping runtime resource and Semu® software to deliver highest debug productivity, VeriTiger-V9P can significantly reduce the digital IC development time.

Hardware

FPGA Information

- Xilinx Virtex UltraScale+ XCVU9P FPGA
- 15.5 Million Estimated ASIC Gates
- 2586K System Logic Cells
- FPGA Memory 345.9Mb
  (Block RAM 75.9Mb+Ultra RAM 270Mb)
- 6840 DSP Slices

Clock Resources

- 4 Programmable Differential Clocks
- 2 Clocks at 20MHz, 2 Clocks at 27MHz
- 2 SI5338 MMCX Differential Clock Inputs
- 1 SI5338 MMCX Differential Clock Output
- 2 MGT Differential Clocks at 100MHz
- Direct Connect-to FPGA Differential Clocks Offered By 2 Pairs of MMCX
- 3 Transceiver Refclks at 100MHz
- 1 Multi-FPGA Shared and Global Programmable Differential ZCLK Clocks

Connector Resources

- 6 HSPI2-MGT Connectors, Offering 40 Lanes GTY Channel
- 2 QSFP Interfaces, Offering 8 Lanes GTY Channel
- 8 HSPI2-DQS Connectors
- 3 HSPI2-CAC Connectors, Supporting 3 DDR3/DDR4
- 3 HSPI2-LVDS Connectors, Offering71 LVDS Differential Pairs
- 720 High-performance I/Os in total in HSPI2 Connectors
- 2 Independent Buttons, 1 Four-digit DIP Switch, 4 User-defined LED Lights

Platform Parameters

- Dimensions: L223mm, W340mm, H91mm
- Weight: 3.0 Kg
- Max Power Consumption: 120W

Software

System Monitoring

- Monitor Voltage and Current
- Monitor FPGA Temperature
- Monitor Daughter Cards States
- Auto Fan Speed Adjustment and Support Mute Mode

Support Multiple Loading Modes

- USB-JTAG Mode
- Ethernet-Selected Map Mode
- SDCard Configuration

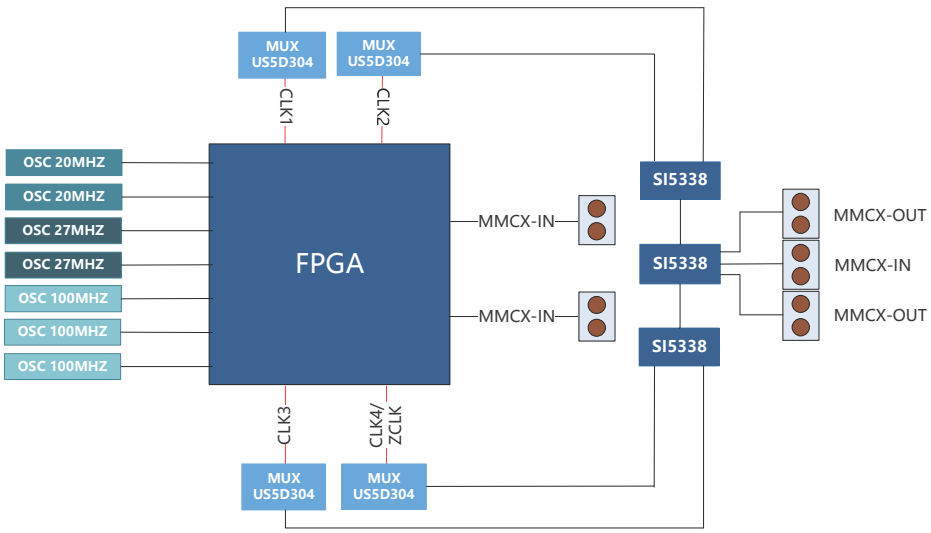
Deep Debug

- Support Virtual Pins for Debug Signal Capturing
- Support Deep Debug, Waveform Trigger and Display
- Semu® Software to Deliver Highest Debug Productivity

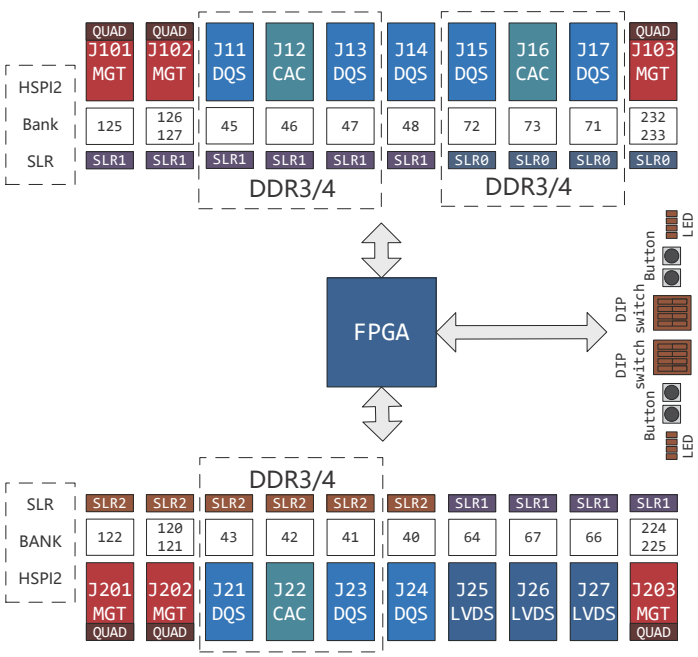
Resources Management

- Support Suits Management
- Support Hardware Self-test

Clock Architecture



I/O Architecture



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