VeriTiger®-QV19P

HyperSilicon® 亞科鴻禹

VeriTiger®-QV19P is the latest generation of prototyping system from HyperSilicon, using Xilinx Virtex UltraScale+ XCVU19P FPGA which provides the highest logic density and I/O count on a single device ever built by Xilinx. VeriTiger-QV19P delivers higher performance, faster running speed and more flexible scalability to accelerate software development, system verification and validation. Through the Protowizard® software to manage prototyping runtime resource and Semu® software to deliver highest debug productivity, VeriTiger-QV19P can dramatically reduce the time-to-tapeout (TTT) pressure of digital IC design.

Hardware

FPGA Information

- 4 Xilinx Virtex UltraScale+ XCVU19P FPGAs
- 196 Million Estimated ASIC Gates
- 35752K System Logic Cells
- FPGA Memory 663.6Mb (Block RAM 303.6Mb+Ultra RAM 360Mb)
- 15360 DSP Slices

Clock Resources

- 40 Programmable Differential Clocks
- 16 MGT Differential Clocks at 100MHz
- 4 Single-ended Clocks at 20MHz, 4 Single-ended Clocks at 27MHz
- 16 Programmable Differential Clock Outputs on Front Panel
- 8 Global Programmable Differential ZCLK Clocks
- 8 Programmable Global Control SCLK Clocks

Connector Resources

- 16 HSPI2-MGT Connectors, Offering 128 Lanes GTY Channel
- 8 QSFP Interfaces, Offering 32 Lanes GTY Channel
- 16 HSPI2-DQS Connectors
- 16 HSPI2-CAC Connectors
- 96 HSPI2-LVDS Connectors, Offering 2296 LVDS Differential Pairs
- 6576 High-performance I/Os in total in HSPI2 Connectors
- 8 QTH-MGT Connectors, Offering 16 Lanes GTY Channel and 96 Single-ended I/Os
- 8 DDR4 SO-DIMMs on top panel, supporting 72bit ECC, providing up to 128GB of memory, and running at 2,400Mbps most
- 16 Independent Buttons, 8 Four-digit DIP Switches, 32 User-defined LED Lights

Platform Parameters

- Dimensions: L444mm, W678mm, H95mm
- Weight: 13.6 Kg
- Max Power Consumption: 560W

Software

System Monitoring

- Monitor Voltage and Current
- Monitor System Running States
- Monitor FPGA Temperature
- Monitor Daughter Cards States
- Auto Power Off on Overvoltage or Overcurrent
- Auto Fan Speed Adjustment and Support Mute Mode

Support Multiple Loading Modes

- USB-JTAG Mode
- USB-Selected Map Mode
- Ethernet-JTAG Mode
- Ethernet-Selected Map Mode
- SDCard Configuration

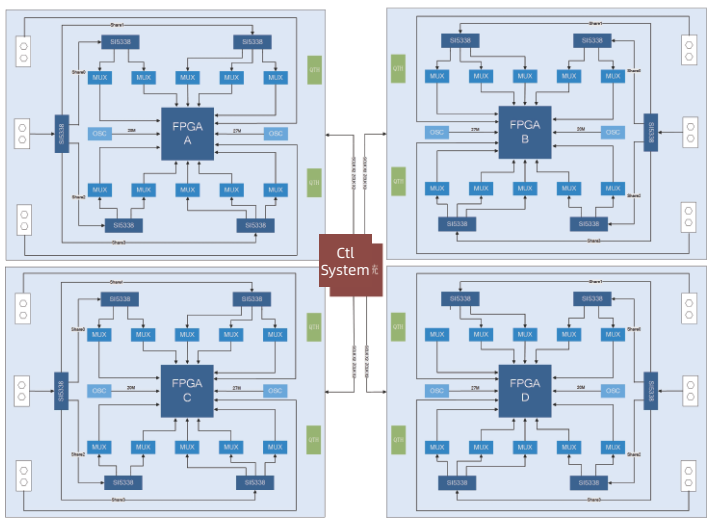
Deep Debug

- Support Virtual Pins for Debug Signal Capturing
- Support the Reset of the Daughter Cards
- Support Deep Debug, Waveform Trigger and Display
- Support EDIF Partition and System-lever Timing Analysis
- Semu® Software to Deliver Highest Debug Productivity

Resources Management

- ProtoWizard® software for Multi-design and Multi-user
- Support Multi-VeriTiger-V19P Systems Management
- Administrator Permission
- Support Suit and Communication Encryption
- Support Online Firmware Update
- Support Hardware Self-test
- HyperDman Software for Daughter Cards Management

Clock Architecture



I/O Architecture

11-12 Floor, Yankuang Xinda Building, No.66 Danshan Road, Xishan District, Wuxi, China
Tel: +86-510-6808 8508 Fax: +86-510-6885 2366 P.C. : 214105 www.hypersilicon.com