VeriTiger®-K115

HyperSilicon® 亞科鴻禹

VeriTiger®-K115 is a pretty agile and easy bring-up prototyping system from HyperSilicon, using Xilinx Kintex UltraScale XCKU115 FPGA. VeriTiger-K115 delivers high performance, fast running speed and flexible scalability to accelerate software development, system verification and validation. Through the Protowizard® software to manage prototyping runtime resource and Semu® software to deliver highest debug productivity, VeriTiger-K115 can significantly reduce the digital IC development time.

Hardware

FPGA Information

- Xilinx Kintex UltraScale XCKU115 FPGA
- 7 Million Estimated ASIC Gates
- 1451K System Logic Cells
- 75.9Mb Total Block RAM
- 5520 DSP Slices

Clock Resources

- 4 Programmable Differential Clocks
- 2 Clocks at 20MHz, 2 Clocks at 27MHz
- 2 SI5338 MMCX Differential Clock Inputs
- 1 SI5338 MMCX Differential Clock Output
- Direct Connect-to FPGA Differential Clocks Offered By 2 Pairs of MMCX
- 3 Transceiver Refclks at 100MHz
- 1 Multi-FPGA Shared and Global Programmable Differential ZCLK Clocks

Connector Resources

- 7 HSPI2-MGT Connectors, Offering 52 Lanes GTH Channel
- 2 QSFP Interfaces, Offering 8 Lanes GTH Channel
- 6 HSPI2-DQS Connectors
- 3 HSPI2-CAC Connectors, Supporting 3 DDR3/DDR4
- 2 HSPI2-LVDS Connectors, Offering 47 LVDS Pairs
- 1 HSPI2-SEND Connector, supporting 3.3V voltage
- 616 High-performance I/Os in total in HSPI2 Connectors
- 4 Separate Buttons, 2 Four-digit DIP Switch, 8 User-defined LED Lights

Platform Parameters

- Dimensions: L340mm, W223mm, H91mm
- Weight: 3.0 Kg
- Max Power Consumption: 120W

Software

System Monitoring

- Monitor Voltage and Current
- Monitor FPGA Temperature
- Monitor Daughter Cards States
- Auto Fan Speed Adjustment and Support Mute Mode

Support Multiple Loading Modes

- USB-JTAG Mode
- Ethernet-Selected Map Mode
- SDCard Configuration

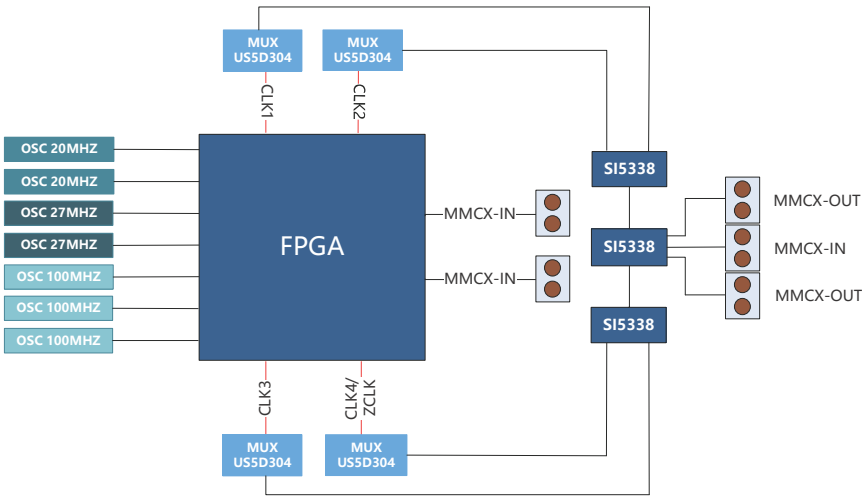
Deep Debug

- Support Virtual Pins for Debug Signal Capturing
- Support Deep Debug, Waveform Trigger and Display
- Semu® Software to Deliver Highest Debug Productivity

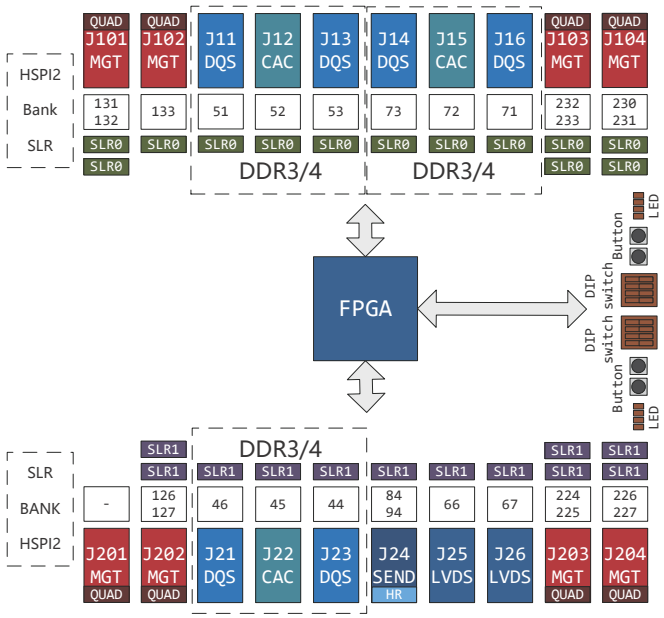
Resources Management

- Support Suits Management
- Support Hardware Self-test

Clock Architecture



I/O Architecture



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