VeriTiger®-DV19P

HyperSilicon® 亞科鴻禹

VeriTiger®-DV19P is the latest generation of prototyping system from HyperSilicon, using Xilinx Virtex UltraScale+XCVU19P FPGA which provides the highest logic density and I/O count on a single device ever built by Xilinx. VeriTiger-DV19P delivers higher performance, faster running speed and more flexible scalability to accelerate software development, system verification and validation. Through the Protowizard® software to manage prototyping runtime resource and Semu® software to deliver highest debug productivity, VeriTiger-DV19P can dramatically reduce the time-to-tapeout (TTT) pressure of digital IC design.

Hardware

FPGA Information

- 2 Xilinx Virtex UltraScale+ XCVU19P FPGAs
- 98 Million Estimated ASIC Gates
- 17876K System Logic Cells
- FPGA Memory 331.8Mb
  (Block RAM 151.8Mb+Ultra RAM 180Mb)
- 7680 DSP Slices

Clock Resources

- 20 Programmable Differential Clocks
- 8 MGT Differential Clocks at 100MHz
- 2 Single-ended Clocks at 20MHz, 2 Single-ended Clocks at 27MHz
- 8 Programmable Differential Clock Outputs on Front Panel
- 4 Global Programmable Differential ZCLK Clocks
- 4 Programmable Global Control SCLK Clocks

Connector Resources

- 8 HSPI2-MGT Connectors, Offering 64 Lanes GTY Channel
- 4 QSFP Interfaces, Offering 16 Lanes GTY Channel
- 8 HSPI2-DQS Connectors
- 8 HSPI2-CAC Connectors
- 48 HSPI2-LVDS Connectors, Offering 1148 LVDS Differential Pairs
- 3288 High-performance I/Os in total in HSPI2 Connectors
- 4 QTH-MGT Connectors, Offering 8 Lanes GTY Channel and 48 Single-ended I/Os
- 4 DDR4 SO-DIMMs on top panel, supporting 72bit ECC, providing up to 64GB of memory, and running at 2,400Mbps most
- 8 Independent Buttons, 4 Four-digit DIP Switches, 16 User-defined LED Lights

Platform Parameters

- Dimensions: L447mm, W340mm, H95mm
- Weight: 6.8 Kg
- Max Power Consumption: 300W

Software

System Monitoring

- Monitor Voltage and Current
- Monitor System Running States
- Monitor FPGA Temperature
- Monitor Daughter Cards States
- Auto Power Off on Overvoltage or Overcurrent
- Auto Fan Speed Adjustment and Support Mute Mode

Support Multiple Loading Modes

- USB-JTAG Mode
- USB-Selected Map Mode
- Ethernet-JTAG Mode
- Ethernet-Selected Map Mode
- SDCard Configuration

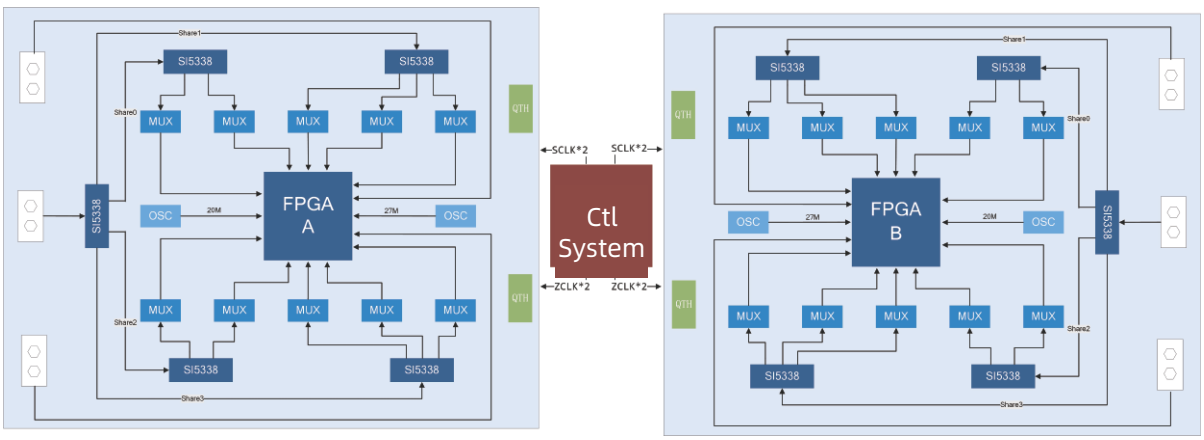
Deep Debug

- Support Virtual Pins for Debug Signal Capturing
- Support the Reset of the Daughter Cards
- Support Deep Debug, Waveform Trigger and Display
- Support EDIF Partition and System-lever Timing Analysis
- Semu® Software to Deliver Highest Debug Productivity

Resources Management

- ProtoWizard® software for Multi-design and Multi-user
- Support Multi-VeriTiger-V19P Systems Management
- Administrator Permission
- Support Suit and Communication Encryption
- Support Online Firmware Update
- Support Hardware Self-test
- HyperDman Software for Daughter Cards Management

Clock Architecture



I/O Architecture